CPU Profile

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CPU Profile

1 Scope

The DCIM CPU Profile describes the properties and interfaces for executing system management tasks related to the management of processors within a system. The profile standardizes and aggregates the description for the CPU properties into a CPU view representation as well as provides static methodology for the clients to query the CPU views without substantial traversal of the model.

2 Normative References

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

DMTF DSP1033, *Profile Registration Profile 1.0.0*

DMTF DSP0226, *Web Services for Management (WS-Management) Specification 1.1.0*

DMTF DSP0227, *WS-Management CIM Binding Specification 1.0.0*

3 Terms and Definitions

For the purposes of this document, the following terms and definitions apply.

3.1

conditional

indicates requirements to be followed strictly in order to conform to the document when the specified conditions are met

3.2

mandatory

indicates requirements to be followed strictly in order to conform to the document and from which no deviation is permitted

3.3

may

indicates a course of action permissible within the limits of the document

3.4

optional

indicates a course of action permissible within the limits of the document

3.5

referencing profile

indicates a profile that owns the definition of this class and can include a reference to this profile in its "Related Profiles" table

3.6
shall
indicates requirements to be followed strictly in order to conform to the document and from which no deviation is permitted

3.7
FQDD
Fully Qualified Device Descriptor is used to identify a particular component in a system.

3.8
Interop Namespace
Interop Namespace is where instrumentation instantiates classes to advertise its capabilities for client discovery.

3.9
Implementation Namespace
Implementation Namespace is where instrumentation instantiates classes relevant to executing core management tasks.

3.10
ENUMERATE
Refers to WS-MAN ENUMERATE operation as described in Section 8.2 of DSP0226_V1.1 and Section 9.1 of DSP0227_V1.0

3.11
GET
Refers to WS-MAN GET operation as defined in Section 7.3 of DSP00226_V1.1 and Section 7.1 of DSP0227_V1.0

4 Symbols and Abbreviated Terms

4.1
CIM
Common Information Model

4.2
iDRAC
Integrated Dell Remote Access Controller – management controller for blades and monolithic servers

4.3
CMC
Chassis Manager Controller – management controller for the modular chassis

4.4
WBEM
Web-Based Enterprise Management

5 Synopsis

Profile Name: CPU

Version: 1.0.0

Organization: Dell

CIM Schema Version: 2.21.0 Experimental

Dell Schema Version: 1.0.0

Interop Namespace: root/interop

Implementation Namespace: root/dcim

Central Class: DCIM_CPUView

Scoping Class: DCIM_ComputerSystem

The Dell CPU Profile is a component profile that contains the Dell specific implementation requirements for CPU view.

DCIM_CPUView shall be the Central Class.

Table 1 identifies profiles that are related to this profile.

Table 1 – Related Profiles

Profile Name	Organization	Version	Relationship
None			

6 Description

The Dell CPU Profile describes platform's CPUs. Each CPU's information is represented by an instance of DCIM_CPUView class.

Figure 1 details typical Dell CPU Profile implementation for a platform containing two CPUs. In order for client to discover the instrumentation's support of this profile, CPUProfile is instantiated in the Interop Namespace. CPUProfile instance describes the information about the implemented profile: most importantly, the name and version of the profile and the organization name that produced the profile.

CPU1 and CPU2 are the CPU views representing the two CPUs in the Implementation Namespace. They are associated to the Interop namespace's CPUProfile instance.

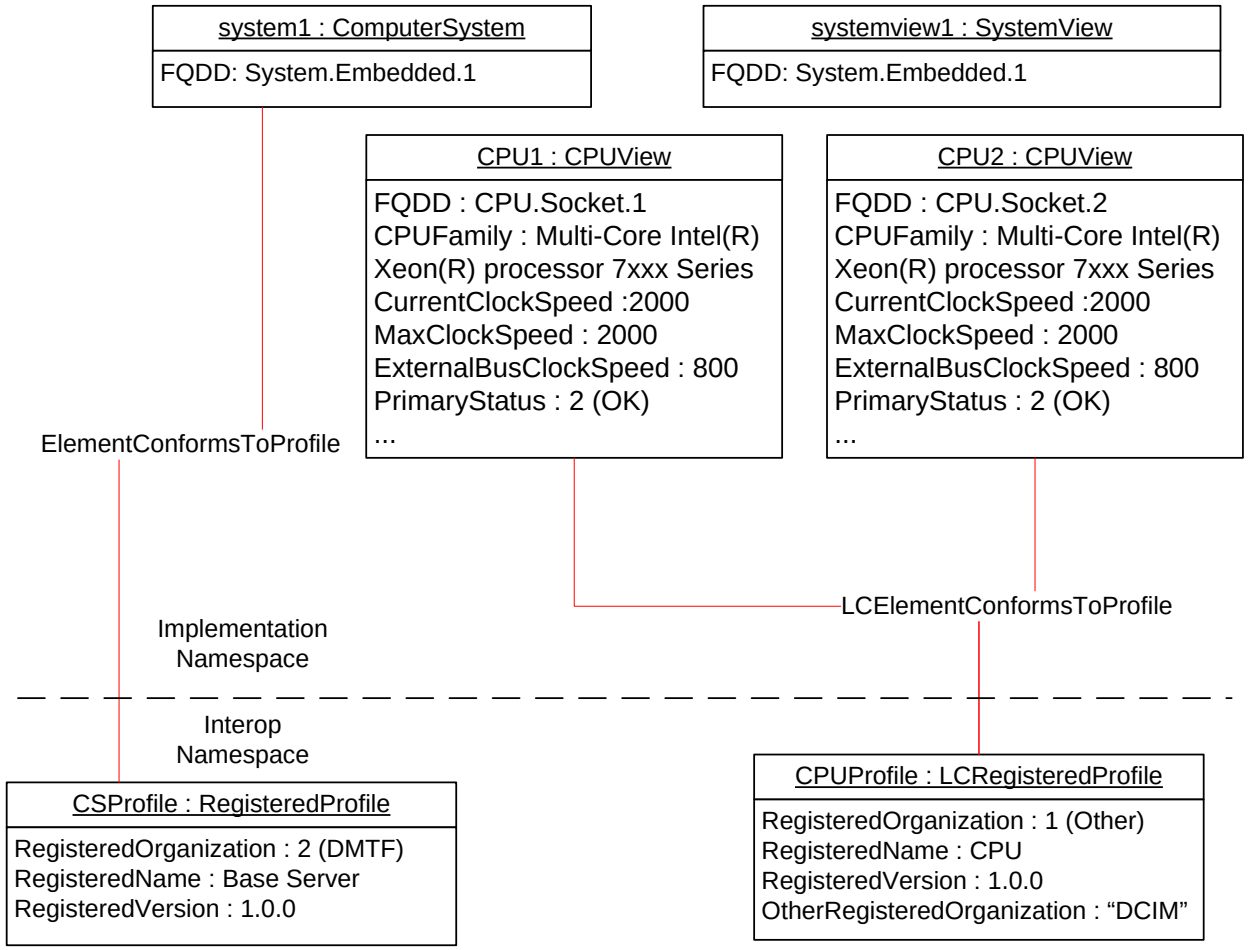

Figure 1 – CPU Profile Implementation

7 Implementation Description

This section describes the requirements and guidelines for implementing Dell CPU Profile.

Table 2 –Class Requirements: CPU Profile

Element Name	Requirement	Description
Classes		
DCIM_CPUView	Mandatory	The class shall be implemented in the Implementation Namespace. See section 7.1.
DCIM_LCElementConformsToProfile	Mandatory	The class shall be implemented in the *Implementation Namespace*.
DCIM_LCElementConformsToProfile	Mandatory	The class shall be implemented in the *Interop Namespace*.
DCIM_LCRegisteredProfile	Mandatory	The class shall be implemented in the Interop Namespace. See section 7.2.
Indications		
None defined in this profile		

7.1 CPU View

This section describes the implementation for the DCIM_CPUView class.

This class shall be instantiated in the Implementation Namespace.

The DCIM_ElementConformsToProfile association(s) shall reference the DCIM_CPUView instance(s).

7.1.1 WBEM URIs for WinRM®

The class WBEM URI shall be “http://schemas.dell.com/wbem/wscim/1/cim-schema/2/DCIM_CPUView?__cimnamespace=<Implementation Namespace>”

The key property shall be the InstanceID.

The instance WBEM URI for DCIM_CPUView instance shall be:
“http://schemas.dell.com/wbem/wscim/1/cim-schema/2/DCIM_CPUView?__cimnamespace=<Implementation Namespace>+InstanceID=<FQDD>”

7.1.2 Operations

The following table details the implemented operations on DCIM_CPUView.

Table 3 – DCIM_CPUView - Operations

Operation Name	Requirements	Required Input
Get	Mandatory	Instance URI
Enumerate	Mandatory	Class URI

7.1.3 Properties

The following table details the implemented properties for DCIM_CPUView instance representing a processor in a system. The “Requirements” column shall denote the implementation requirement for the corresponding property. If the column “Property Name” matches the property name, the property either shall have the value denoted in the corresponding column “Additional Requirement”, or shall be implemented according to the requirements in the corresponding column “Additional Requirement”.

Table 4 – DCIM_CPUView - Properties

Property Name	Requirements	Type	Requirement and Description
InstanceID	Mandatory	string	The property value shall be the FQDD property value.
FQDD	Mandatory	string	A string containing the Fully Qualified Device Description a user-friendly name for the object.
CPUFamily	Mandatory	string	The Processor family type.
CurrentClockSpeed	Mandatory	uint32	The property value shall be in MHz. The current speed (in MHz) of this Processor.
MaxClockSpeed	Mandatory	uint32	The property value shall be in MHz. The maximum speed (in MHz) of this Processor.
ExternalBusClockSpeed	Mandatory	uint32	The property value shall be in MHz. The speed (in MHz) of the external bus interface (known as the front side bus).
PrimaryStatus	Mandatory	uint32	PrimaryStatus provides a high level status value, intended to align with Red-Yellow-Green type representation of status.
NumberofEnabledThreads	Mandatory	uint16	Total number of hardware enabled threads for processor. NOTE: The disabling of the multithreading by the BIOS does not affect the number of hardware enabled threads reported by this property.
NumberofEnabledCores	Mandatory	uint32	Number of processor cores enabled for processor.
NumberOfProcessorCores	Mandatory	uint32	Number of processor cores available for processor.
Voltage	Mandatory	string	The voltage(s) of the processor.
CPUStatus	Mandatory	uint16	Indicates the current status of the Processor. For example, the Processor might be disabled due to a POST error (value=3).
Characteristics[]	Mandatory	uint32	The characteristics include certain features of the processor such as 64 bit support for data width of the processor.
Model	Mandatory	string	The make and or model of the product
Manufacturer	Mandatory	string	The name of the organization responsible for producing the processor.
Cache1Level	Mandatory	uint16	The cache level for Cache1 labeled cache.
Cache2Level	Mandatory	uint16	The cache level for Cache1 labeled cache.
Cache3Level	Mandatory	uint16	The cache level for Cache1 labeled cache.
Cache1Size	Mandatory	uint64	in Kbytes. The total memory size of the cache in KBytes.
Cache2Size	Mandatory	uint64	in Kbytes. The total memory size of the cache in KBytes.
Cache3Size	Mandatory	uint64	in Kbytes. The total memory size of the cache

			in KBytes.
Cache1PrimaryStatus	Mandatory	uint32	Cache1PrimaryStatus provides a high level status value, intended to align with Red-Yellow-Green type representation of status.
Cache2PrimaryStatus	Mandatory	uint32	Cache2PrimaryStatus provides a high level status value, intended to align with Red-Yellow-Green type representation of status.
Cache3PrimaryStatus	Mandatory	uint32	Cache3PrimaryStatus provides a high level status value, intended to align with Red-Yellow-Green type representation of status.
Cache1ErrorMethodology	Optional	uint16	Cache ErrorMethodology - Contains the enumerated value that describes the cache's error detection/correction mechanism
Cache2ErrorMethodology	Optional	uint16	Cache ErrorMethodology - Contains the enumerated value that describes the cache's error detection/correction mechanism
Cache3ErrorMethodology	Optional	uint16	Cache ErrorMethodology - Contains the enumerated value that describes the cache's error detection/correction mechanism
Cache1WritePolicy	Mandatory	uint16	Defines whether this is write-back (value=1) or write-through (value=0) Cache, or whether this information \"Varies with Address\" (2) or \"Unknown\" (3) can be specified.
Cache2WritePolicy	Mandatory	uint16	Defines whether this is write-back (value=1) or write-through (value=0) Cache, or whether this information \"Varies with Address\" (2) or \"Unknown\" (3) can be specified.
Cache3WritePolicy	Mandatory	uint16	Defines whether this is write-back (value=1) or write-through (value=0) Cache, or whether this information \"Varies with Address\" (2) or \"Unknown\" (3) can be specified.
Cache1Type	Mandatory	uint16	Defines whether this is for instruction caching (value=3), data caching (value=4) or both (value=5, \"Unified\"). Also, \"Other\" (1) and \"Unknown\" (2) can be defined.
Cache2Type	Mandatory	uint16	Defines whether this is for instruction caching (value=3), data caching (value=4) or both (value=5, \"Unified\"). Also, \"Other\" (1) and \"Unknown\" (2) can be defined.
Cache3Type	Mandatory	uint16	Defines whether this is for instruction caching (value=3), data caching (value=4) or both (value=5, \"Unified\"). Also, \"Other\" (1) and \"Unknown\" (2) can be defined.
Cache1Associativity	Mandatory	uint16	An integer enumeration defining the system cache associativity.
Cache2Associativity	Mandatory	uint16	An integer enumeration defining the system cache associativity.
Cache3Associativity	Mandatory	uint16	An integer enumeration defining the system cache associativity.
Cache1SRAMType	Mandatory	uint16	Cache SRAM Type.
Cache2SRAMType	Mandatory	uint16	Cache SRAM Type.
Cache3SRAMType	Mandatory	uint16	Cache SRAM Type.
LastSystemInventoryTime	Mandatory	string	This property provides the last time \"System \"Inventory Collection On Reboot(CSIOR)\" was performed. The value is represented as

			yyyymmddHHMMSS.
LastUpdateTime	Mandatory	string	This property provides the last time the data was updated. The value is represented as yyyymmddHHMMSS

7.2 CPU Profile Profile Registration

This section describes the implementation for the DCIM_LCRegisteredProfile class.

This class shall be instantiated in the Interop Namespace.

The DCIM_ElementConformsToProfile association(s) shall reference the DCIM_LCRegisteredProfile instance.

7.2.1 WBEM URIs for WinRM®

The class WBEM URI shall be "http://schemas.dmtf.org/wbem/wscim/1/cim-schema/2/CIM_RegisteredProfile?__cimnamespace=<Interop Namespace>"

The key property shall be the InstanceID property.

The instance WBEM URI shall be: “http://schemas.dell.com/wbem/wscim/1/cim-schema/2/DCIM_LCRegisteredProfile?__cimnamespace=<InteropNamespace>+InstanceID=DCIM:CPU:1.0.0”

7.2.2 Operations

The following table details the implemented operations on DCIM_LCRegisteredProfile.

Table 5 – DCIM_LCRegisteredProfile - Operations

Operation Name	Requirements	Required Input
Get	Mandatory	Instance URI
Enumerate	Mandatory	Class URI

7.2.3 Properties

The following table details the implemented properties for DCIM_LCRegisteredProfile instance representing CPU Profile implementation. The “Requirements” column shall denote the implementation requirement for the corresponding property. If the column “Name” matches the property name, the property either shall have the value denoted in the corresponding column “Additional Requirements”, or shall be implemented according to the requirements in the corresponding column “Additional Requirements”.

Table 6 – DCIM_LCRegisteredProfile

Property Name	Requirement	Additional Requirements
InstanceID	Mandatory	DCIM:CPU:1.0.0
RegisteredName	Mandatory	This property shall have a value of "CPU".
RegisteredVersion	Mandatory	This property shall have a value of "1.0.0".
RegisteredOrganization	Mandatory	This property shall have a value of 1 (Other).
OtherRegisteredOrganization	Mandatory	The property value shall match “DCIM”.

8 Methods

This section details the requirements for supporting extrinsic methods for the CIM elements defined by this profile.

No additional details specified.

9 Use Cases

This section contains use cases for the Dell CPU Profile. For the general instance and class URI structure, see section 7.1.1 and 7.2.1**,** respectively.

Note that URIs in this section are in form of WBEM URIs for WinRM®.

9.1 Discovery of CPU profile support

Use one of the two procedures below to confirm the existence of CPU profile support

A) GET the *DCIM_LCRegisteredProfile* instance using an *InstanceID* of DCIM:CPU:1.0.0. See Section 3.11 for a definition of GET **.**

Instance URI:

http://schemas.dmtf.org/wbem/wscim/1/cim-schema/2/DCIM_LCRegisteredProfile?__cimnamespace=root/interop+InstanceID=DCIM:CPU:1.0.0

Results for the *InstanceID* of DCIM:CPU:1.0.0 shown below. If no instance is returned, the profile is not supported.

DCIM_LCRegisteredProfile
AdvertiseTypeDescriptions = WS-Identify, Interop Namespace
AdvertiseTypes = 1, 1
InstanceID = DCIM:CPU:1.0.0
OtherRegisteredOrganization = DCIM
RegisteredName = CPU
RegisteredOrganization = 1
RegisteredVersion = 1.0.0

B) ENUMERATE the *CIM_RegisteredProfile* class. See section 3.10 for a definition of ENUMERATE .

Class URI:

http://schemas.dmtf.org/wbem/wscim/1/cim-schema/2/CIM_RegisteredProfile?__cimnamespace=root/interop

Then query the result for the following properties:

RegisteredName = CPU, OtherRegisteredOrganization = DCIM, RegisteredVersion = 1.0.0

9.2 Inventory of CPUs in system

Enumerate the *DCIM_CPUView* class to view all available instances of the class

Class URI:

http://schemas.dell.com/wbem/wscim/1/cim-schema/2/DCIM_CPUView?__cimnamespace=root/dcim

The instance information of all available CPUs will be returned

9.3 Get the first CPU's information

The URI for getting particular instance information is deterministic (i.e the *InstanceID* will be unique for each instance)

For the first CPU in the system, the instance URI will be:

http://schemas.dell.com/wbem/wscim/1/cim-schema/2/DCIM_CPUView?__cimnamespace=root/dcim+InstanceID=CPU.Socket.1

The instance of *DCIM_CPUView* that contains the information on the first CPU will be returned

10 CIM Elements

No additional details specified.

ANNEX A
(informative)

Related MOF Files

Dell Tech Center MOF Library:

http://www.delltechcenter.com/page/DCIM.Library.MOF

Related Managed Object Format (MOF) files:

DCIM_CPUView.mof

DCIM_LCEnumeration.mof

DCIM_LCRegisteredProfile.mof